Novel Process Techniques for Fabricating High Density Trench MOSFETs with Self-Aligned N^+/P^+ Source Formed on the Trench Side Wall

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Abstract. Novel process techniques for fabricating highly dense trench MOSFETs are proposed and verified by experimental and numerical results. P^+ region for p-base contact and N^+ source are formed on the trench side wall by using self-aligned process techniques including triple trench etching. Two-dimensional process and device simulation is performed by using SILVACO with the cell pitch of 1.0 μm for the proposed trench MOSFET. The simulated breakdown voltage and on-resistance are 45 V and 12.9 mΩ·mm², respectively.

INTRODUCTION

Trench gate power MOSFETs are promising devices for power electronics applications such as DC/DC converter, VRM (Voltage Regulator Module), computer peripherals, etc. owing to its high channel density and low on-resistance. Many structures have been studied to reduce the cell pitch of the trench MOSFETs because specific on-resistance is proportional to unit cell area. They have achieved rapid progress in the reduction of the cell pitch of the power MOSFET, especially concentrated on the reduction of the trench width for gate [1].

Recently, trench MOSFET with the trench width of 0.2 μm at the gate edge and the cell pitch of 1.0 μm was reported [2]. The on-resistance and the breakdown of the trench MOSFET were 10 mΩ·mm² and 26 V, respectively. It is also presented that 30 V trench MOSFET with the cell pitch of 1.1 μm showed the on-resistance of 18 mΩ·mm² [3]. However, it becomes more difficult to guarantee enough regions for a good contact because the remained area for source contact becomes very small as the cell pitch reduces to sub-micron range.

We propose novel self-aligned source structure and process techniques for high channel density which will be applicable to sub-micron trench MOSFETs. In this new technique, polysilicon gate is completely buried in the trench and N^+/P^+ source region is formed on the side wall of the silicon trench located upon the trench gate, leaving an enough region for source contacts, as shown in Fig. 1(a). Generally, the minimum cell pitch of the conventional trench MOSFET (Fig. 1b) is limited by the spacer for isolation between polysilicon gate and source even if the contact is opened by self-aligned process. Especially, the portion of the spacer becomes high as the cell pitch reduces to sub-micron ranges. However, the proposed trench MSOFET can secure a large contact size (~0.5 μm) in spite of the reduction in the cell pitch. In this case, contact widths of N^+ or P^+ are determined by the depth of trench.

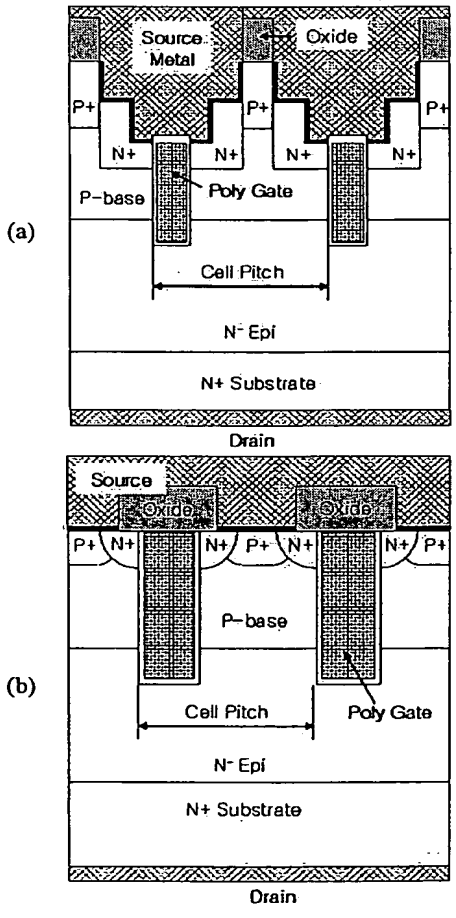


Fig. 1. Cross-sectional views of trench MOSFET. (a) Proposed (b) Conventional

FABRICATION SEQUENCES AND EXPERIMENTAL RESULTS OF KEY STEPS

The self-aligned source structures of the proposed trench MOSFETs are experimentally verified. The important process sequence for fabricating the proposed trench MOSFET using 3 mask layers (trench, poly, and metal) is illustrated in Fig. 2.

A trench etching and implanting process are repeated to form source regions on the sidewall. Starting material is phosphorus doped silicon layer epitaxially grown on top of antimony doped, (100) silicon substrate. The doping concentration and thickness of epitaxial layer are 2e16 cm^{-3} and 7 μm, respectively.

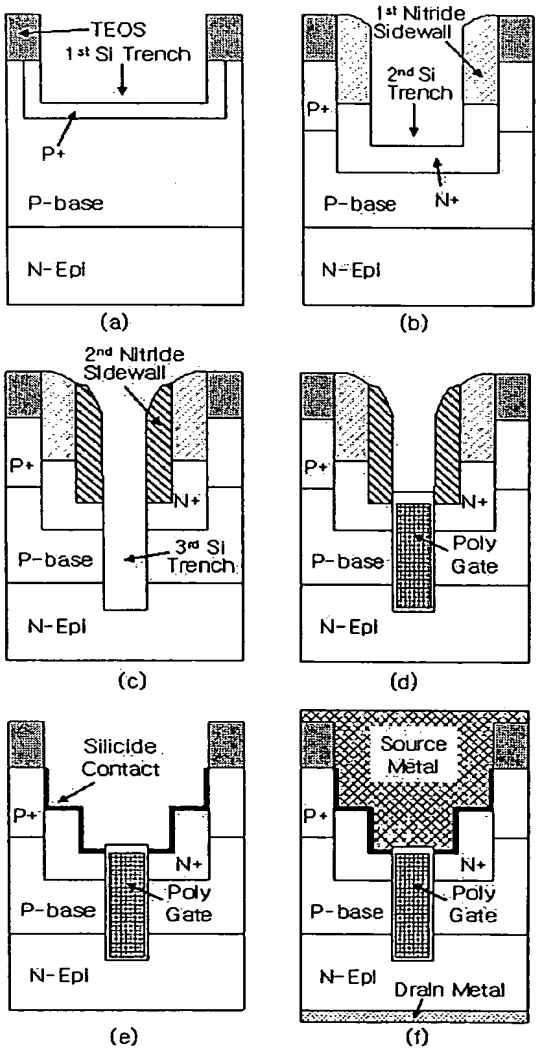
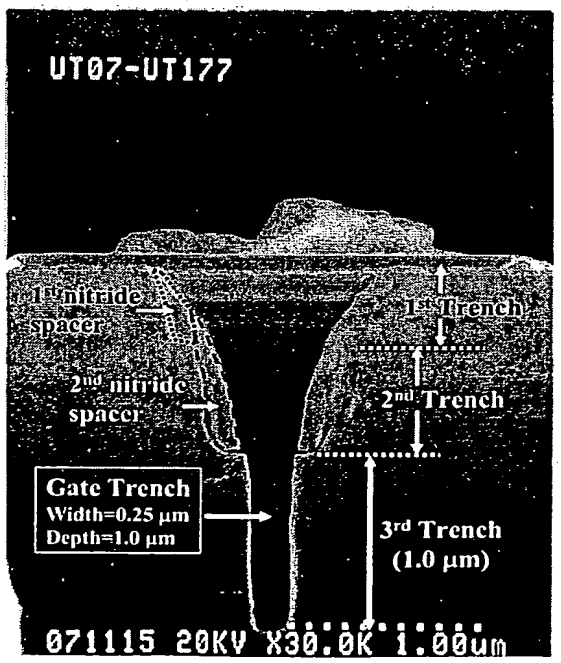


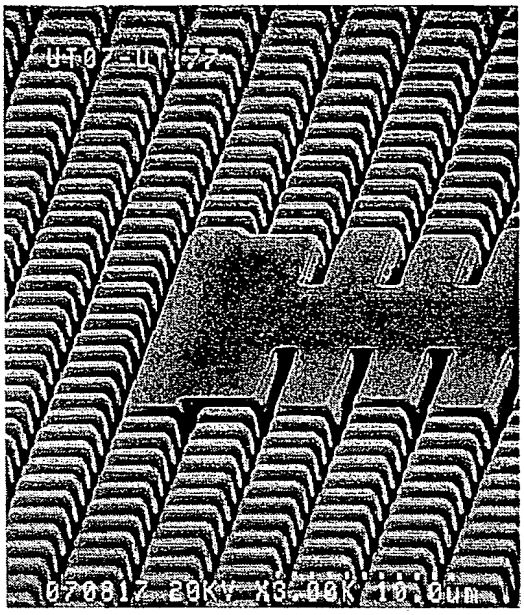
Fig. 2. Proc ss s qu nces of th propos d tr nch MOSFETs.

The key process steps are: (a) p-well formation by implanting boron (2.0e13/cm^2) and annealing followed by 1st silicon trench etching [trench mask] and P^+ source formation by implanting boron (3.7e15/cm^2), (b) 1st nitride spacer formation by deposition and reactive ion etching (RIE) of nitride, 2nd silicon trench etching, N^+ source formation by implanting arsenic (8.0e15/cm^2), (c) 2nd nitride spacer formation and 3rd silicon etching (~1.0 μm) to define trench gate, (d) oxide growth (350 Å) on the sidewall of the trench, deposition of polysilicon to fill the trenches and etch-back of polysilicon to expose N^+/P^+ source region covered by nitride spacers [poly mask], oxidation of polysilicon to isolate polysilicon gate from N^+/P^+ source, (e) removal of nitride spacers and silicide formation, (f) Al deposition and patterning [metal mask]. Formation of N^+ source region and P^+ region for p-base contact, trench etch for gate, and contact open process are performed by using fully self-aligned process. Also, polysilicon regions for both channel gate and gate pad are automatically isolated by oxidation of polysilicon after etch-back with using poly mask layer.

Fig. 3 shows SEM photograph of triple silicon trench by using double nitride spacer. High quality trench etching was carried out by using magnetically enhanced reactive ion etching in an Applied Materials model P-5000 dry etching system. Thin nitride film (500 Å) was deposited and etched by RIE to form 1st nitride spacer.



(a)



(b)

Fig. 3. SEM photograph of the self-aligned triple silicon trench structure for gate and source. 1st and 2nd nitride spacers were used as a masking layer for trench etching the silicon : (a) cross sectional view and (b) top view.

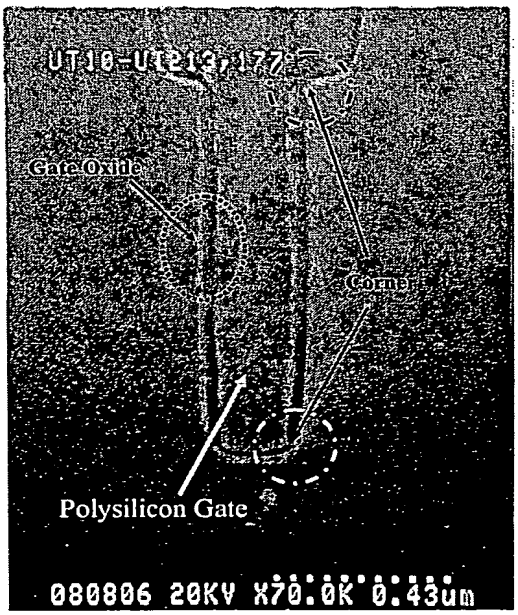


Fig. 4. SEM photograph of trench structur for gat and polysilicon filling with gate oxid of 350 Å.

Exposed silicon region was etched by the thickness of 4,000 ~ 5,000 Å. Formation of 2nd nitride spacer was carried out by the deposition and the etching of thin nitride film (500 Å). The depths of first and second silicon trench determine the source contact area. As shown in Fig. 3(a), narrow trench structure for gate was obtained by dual nitride spacers. The width and the depth of trench structure are 0.25 μm and 1.0 μm, respectively. Fig. 3(b) shows the top view of the trench structure adjacent the edge of the finger for gate electrode. The uniform trench structure is obtained.

Fig. 4 shows the cross-sectional SEM photograph of a filling the trench. The trench structure for DMOSFET was successfully filled with polysilicon with the gate oxide of 350 Å thermally grown on the sidewall. Non-uniform oxide was formed along the trench surface, especially thinner oxide at the corner of the trench, as shown in Fig. 4. However, uniform oxide can be obtained by using trench corner rounding technique [4].

Fig. 5 shows the cross-sectional SEM photograph of the trench gate MOSFET structure prior to metallization with the cell pitch of 2.4 μm. Gate electrode was formed by filling and etching-back of polysilicon. From this photograph, it can be stated that the high density trench MOSFET with the cell pitch of 1.0 μm can be achieved when the source region is formed to have the width of 0.3~0.4 μm. Especially, the contact width of the N^+/P^+ is 0.4~0.5 μm at each side of the trench. It means that the contact width of the source region becomes nearly 1 μm per each cell.

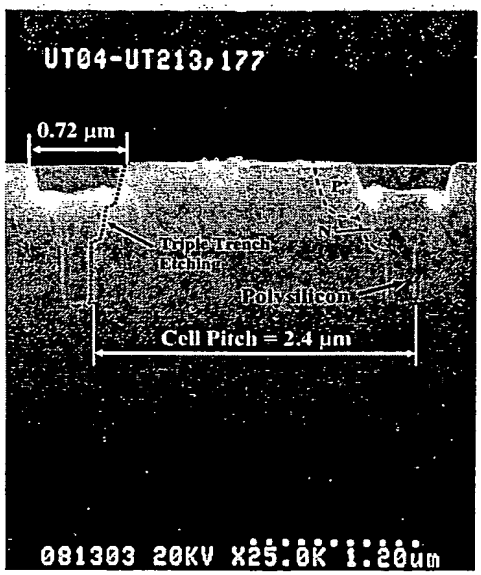


Fig. 5. SEM photograph of the cross-sectional vi w of trench-gat MOSFET structure prior to metallization with the cell pitch of 2.4 μm.

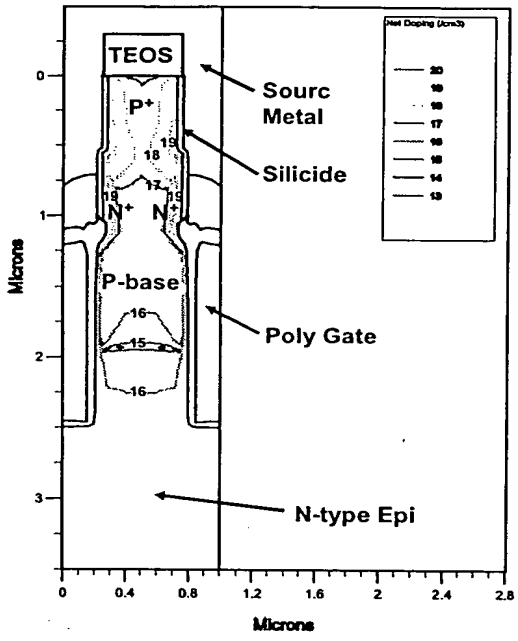


Fig. 6 Doping contours of the proposed trench MOSFETs. N^+ and P^+ region was formed on the sidewall above the recessed polysilicon gate.

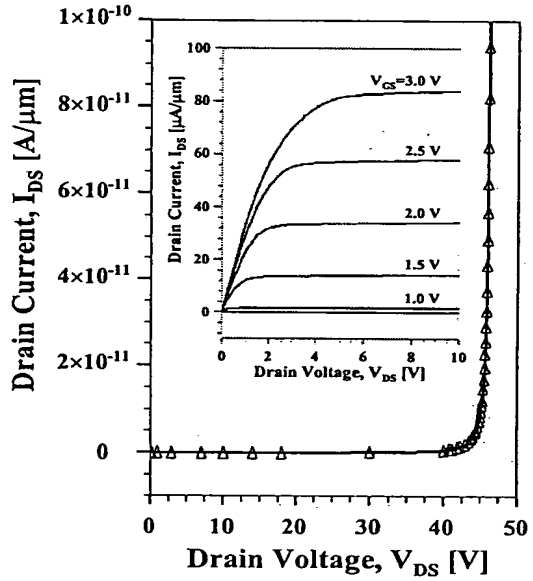


Fig. 7 Breakdown characteristics of the trench MOSFETs when the gate bias is zero (BV=42 V). Inset shows forward I-V characteristics of the proposed trench MOSFET (V_T=0.82 V).

SIMULATION RESULTS

Two dimensional process and device simulation for the proposed trench MOSFETs with a cell pitch of 1.0 μm were performed by using SILVACO. Fig. 6 shows two-dimensional doping contours of the simulated structure. N^+/P^+ source region and channel region were successfully formed on the trench sidewall. The doping concentration of boron for channel is around 5×10^{16} cm^{-3} and threshold voltage is 0.82 V.

Fig. 7 shows simulated breakdown characteristics of the trench MOSFETs with the breakdown voltage of 45 V and inset shows forward I-V characteristics when the gate bias is increased by the increment of 0.5 V from 1.0 V to 3.0 V. Specific on-resistance of this device is 12.9 ~~mΩ·mm~~^{2} when gate and drain voltages are 5 V and 0.1 V, respectively. The proposed trench MOSFET shows good trade-off characteristics between breakdown voltage and specific on-resistance.

CONCLUSIONS

Novel process techniques for fabricating high density trench MOSFETs were presented. The proposed self-aligned source structure gives advantages of fully self-aligned process, security of source contact region, and very high channel density. The contact area for the N^+ source can be easily controlled by the depth of trench etching.

ACKNOWLEDGMENTS

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